DIGITAL SIGNAL GENERATOR FOR EXCITING AN AREA OF ULTRASONIC TRANSDUCERS

Tanase Mihail Eugen[1], Lie Ioan [1], Marinca Bogdan[1], Babaita Mircea[1]

[1] "Politehnica" University of Timisoara, Departments of Communications and of Applied Electronics, Bd. V. Parvan no 2, 300223 Timisoara, Romania.
(e-mails: ioan.lie@etc.utt.ro , mihail.tanase@etc.utt.ro).

Abstract: The authors are part of a larger staff, lead by prof.dr.ing. M.E.Tanase that have, for a long time, studied the optimal ultrasonic investigations in elastic mediums, especially in biological mediums. The digital signal generator of sequence of voltage pulses is part of the imagistic ultrasonic system's structure type B, that is ment to deliver required to excite the ultrasonic transducers. Its parameters are assesed with the program. For the utility of the generator in other working fields, the digital generator was designed and manufactured as a function generator. We expose the principles that we used to conceive the constitutive elements and the results of the material experiments.

Keywords: OCT, USB

1. INTRODUCTION

The method to produce ultrasonic images in B mode is practically the most used, and it is made with areas in phases excited of ultrasonic transducers, where all the elements of the area are active both at the emission and reception of the ultrasonic fascicle. For the excitation of the ultrasonic transducers from the matrix area we use the equipment depicted in figure 1.

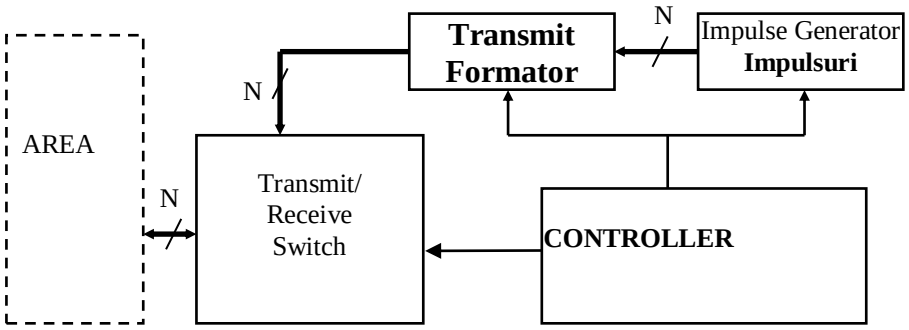

Figure 1. The structure of the equipment used for the excitation of the ultrasonic transducers area

Because of the high value signal/noise ratio and very good spatial and contrast resolution, the investigation techniques with in phase matrix transducers are useful especially in medical imagistics.

The digital signal generator delivers the voltage pulses of frequency , level, number of pulses of the package and the range between the parcels is assesed by the current application. The phasing of the excitation pulses is made by the emission - forming block. Data and the proper phasing are permanently controled by the program through the controller.

2. DISCUSSION AND EXPERIMENTAL RESULTS

The digital signal generator was designed so that it may be used not only for the excitation of the ultrasonic transducers from the AREA –Figure 1, but also in other applications and research (for instance, computer controlled automatic testing of equipment and were board functionality). Considering these, the generator imposed: a) large range adjustment of the output signal amplitude and frequency; b) the possibility to generate a sinusoidal, rectangular and triangular waveform; c) analog and digital controlled outputs; d) TTL/CMOS compatible analog and digital synchronization triggering.

The block structure developed for the digital signal generator is presented in Figure 2.

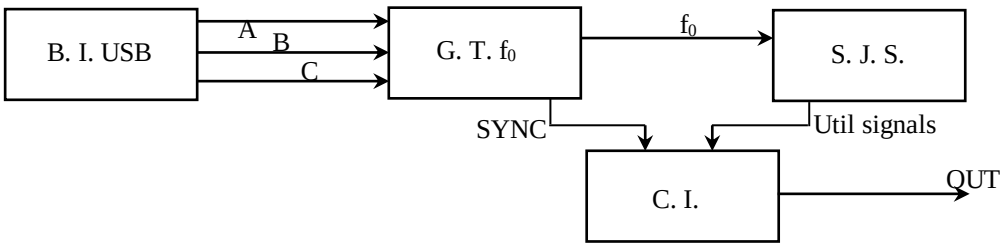

Figure 2. Digital signal generator. Main block diagram.

It was chosen to connect the board of the generator to the USB input / output in order to make the generator available both for a separate central unit PC and for a Laptop PC and also to provide a high working speed with a PC. The clock signal made with the GTf_0 block provide the signal of desired frequency f_0 to the synthesis block BSS which, digital offers the output signal of the requested shape. Through the output circuit CI the specified outputs mentioned at condition (c) are delivered.

The clock generator, with frequency f_0 is made, based on the professional integrated circuit MAX038, and it is indicated, at the block diagram level Figure 3.

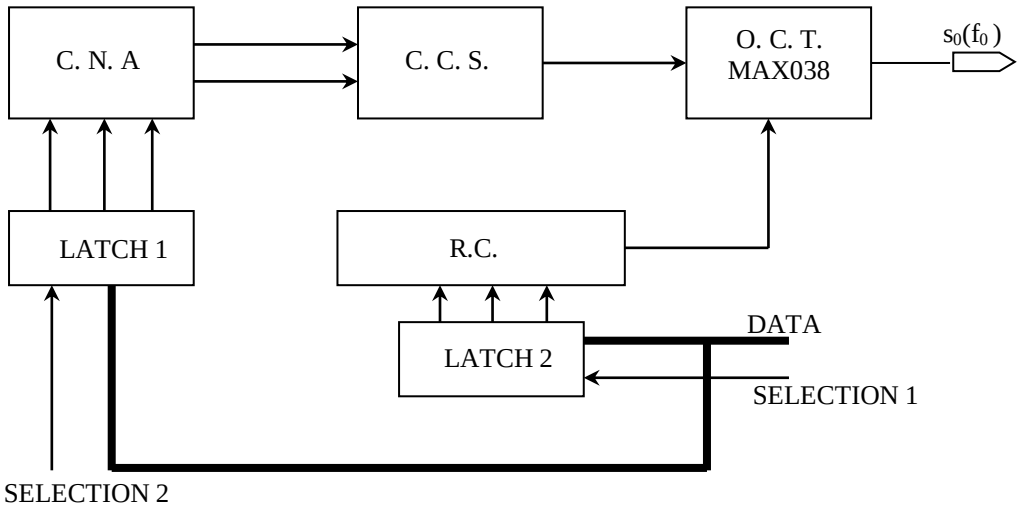

Figure 3. The tact generator with f_0 frequency. The functional block sketch.

The integrated circuit Max038 is a voltage controlled oscillator (VCT) with the operating parameters and current implementation indicated in [3]. The IC forme receives the current $I_{iN} = I_{iNL} + I_{iNR}$ from the signal conditioning block CSS. Through operational amplifiers is delivered I_{iNL} with the main purpose to establish the signal frequency f_0 and

$I_{iNR} = I_{iNL}/16$ for fine adjustment of the frequency f_0.

The integrated circuits and the values of the passive components from the detailed clock generator schematic for $C = 50\text{pF}$ we obtain $f_0 = 28MHz \rightarrow 600KHz$,

for $C = 1500\,pF$ we obtain $f_0 = 1MHz \rightarrow 20KHz$ and

for $C = 30nF$ we obtain $f_0 = 50KHz \rightarrow 1KHz$.

The synthesis signal block, reproduced as a block diagram Figure 4, consists of a complex address generator which controls the reading process of the signal samples that has to be generated from a RAM memory. This memory is previusly written by the PC with the values corresponding to a cycle of the generated signal.

The address generator supplies a also a triggering signal for the synchronizing other external devices on the sampling frequency of the package stored in the RAM memory. The memory is buffered with a blocking counting circuit and clears out at a certain limit address. This is useful because a signal period will always contain less samples than the maximum content capacity which is equal to the capacity of the RAM memory. Thus signal obtained at the output of the circuits will practically be a clean signal.

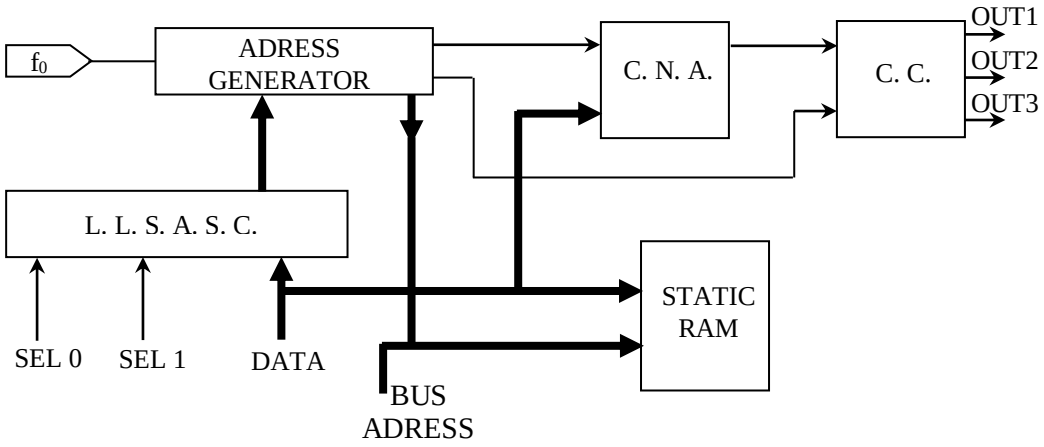

Figure 4.Ssignal block synthesis

3. CONCLUSIONS

The analogically generated signal and the digital generated signal coexists a the corresponding outputs excepted that the signal at the analog output is 2 twice the frequency at the digital output.

In the terms of a frequent use of such a function generator we can use two solutions: the first is designing a dedicated ASIC, and the second, validate case of a restricted use, using a FPGA.

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